

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

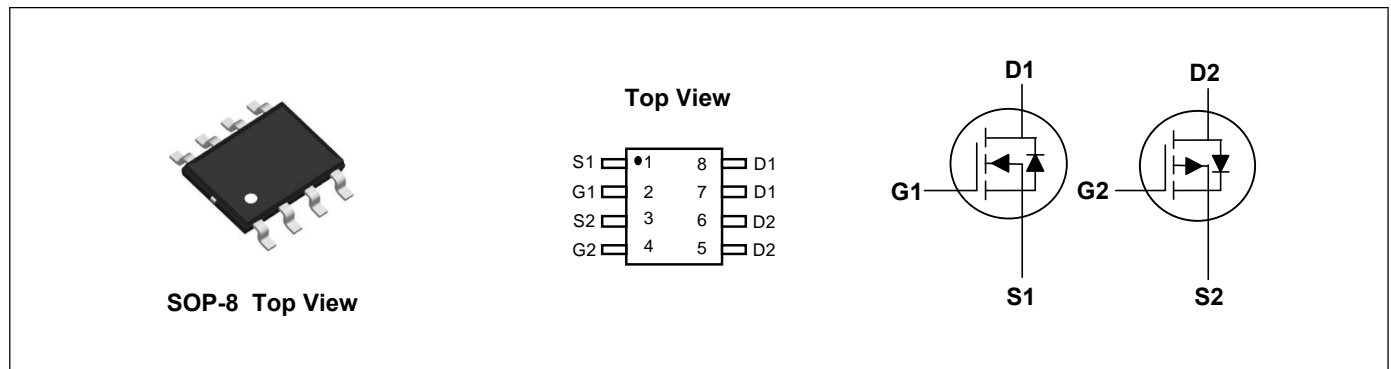
## Applications

- Power management in half bridge and inverters
- DC-DC Converter
- Load Switch

## Product Summary



	N-Ch	P-Ch	
$V_{DS}$	30	-30	V
$I_D$	10	-7.6	A
$R_{DS(ON)}$ (at $V_{GS}=\pm 10V$ )	18	30	m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=\pm 4.5V$ )	28	55	m $\Omega$



## Absolute Maximum Ratings( $T_C=25^\circ C$ , unless otherwise noted)

Parameter	Symbol	N-Ch	P-Ch	Units
Drain-Source Voltage	$V_{DS}$	30	-30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Continuous Drain Current, $V_{GS} @ \pm 10V^1$	$I_{D@T_C=25^\circ C}$	10	-7.6	A
Continuous Drain Current, $V_{GS} @ \pm 10V^1$	$I_{D@T_C=100^\circ C}$	6	-5.9	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	20	-15	A
Single Pulse Avalanche Energy <sup>3</sup>	EAS	22	45	mJ
Avalanche Current	$I_{AS}$	21	-30	A
Total Power Dissipation <sup>4</sup>	$P_{D@T_C=25^\circ C}$	2		W
Storage Temperature Range	$T_{STG}$	-55 to 150		$^\circ C$
Operating Junction Temperature Range	$T_J$	-55 to 150		$^\circ C$

## Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	---	62	$^\circ C/W$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	---	5	$^\circ C/W$

**N-Ch Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	30	---	---	V
BV <sub>DSS</sub> Temperature Coefficient	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Reference to 25°C, I <sub>D</sub> =1mA	---	0.023	---	V/°C
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	---	---	18	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	---	---	28	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	---	2.5	V
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub>		---	-5.2	---	mV/°C
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =24V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10A	---	16	---	S
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	2.5	5	Ω
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	7.2	---	nC
Gate-Source Charge	Q <sub>gs</sub>		---	1.4	---	
Gate-Drain Charge	Q <sub>gd</sub>		---	2.2	---	
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =5A	---	4.1	---	ns
Rise Time	T <sub>r</sub>		---	9.8	---	
Turn-Off Delay Time	T <sub>d(off)</sub>		---	15.5	---	
Fall Time	T <sub>f</sub>		---	6	---	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	572	---	pF
Output Capacitance	C <sub>oss</sub>		---	81	---	
Reverse Transfer Capacitance	C <sub>rss</sub>		---	65	---	

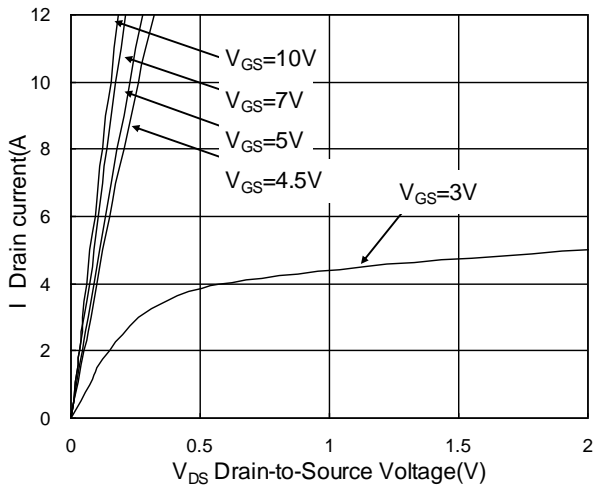
**Drain-Source Diode Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous Source Current <sup>1,5</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	10	A
Pulsed Source Current <sup>2,5</sup>	I <sub>SM</sub>		---	---	20	A
Diode Forward Voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1.2	V

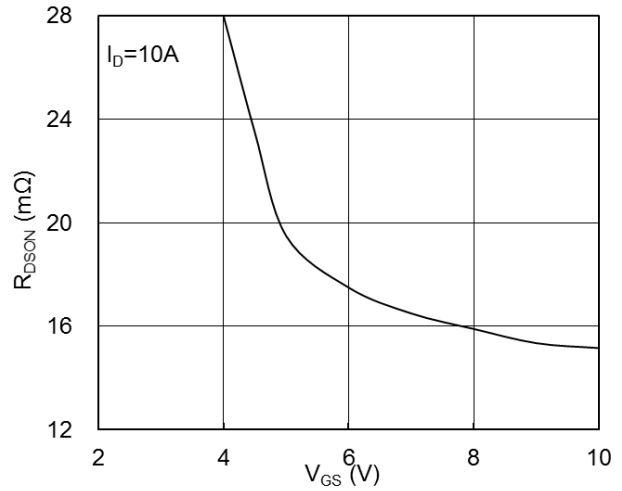
**Note:**

- The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

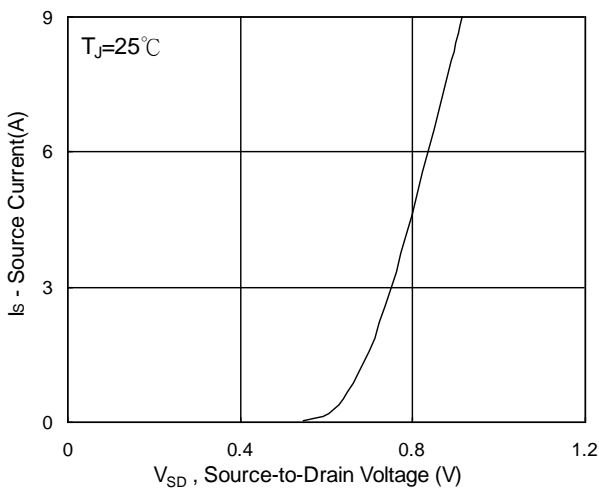
**N-Ch Typical Characteristics**



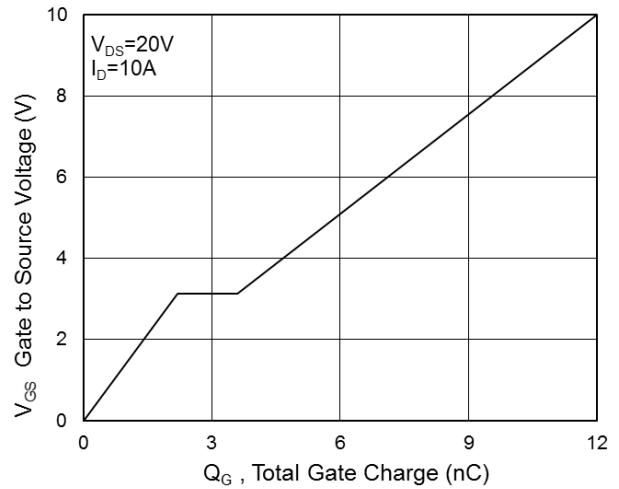
**Fig.1 Typical Output Characteristics**



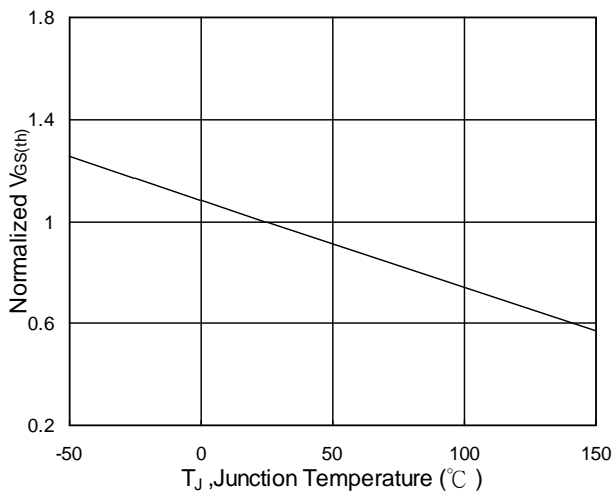
**Fig.2 On-Resistance vs Gate-Source Voltage**



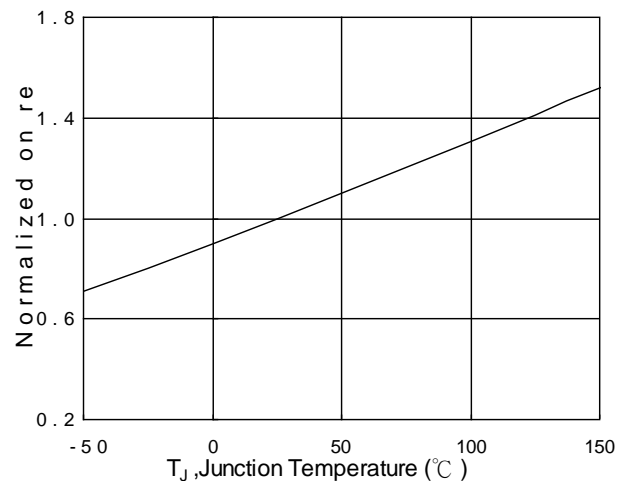
**Fig.3 Forward Characteristics of Reverse**



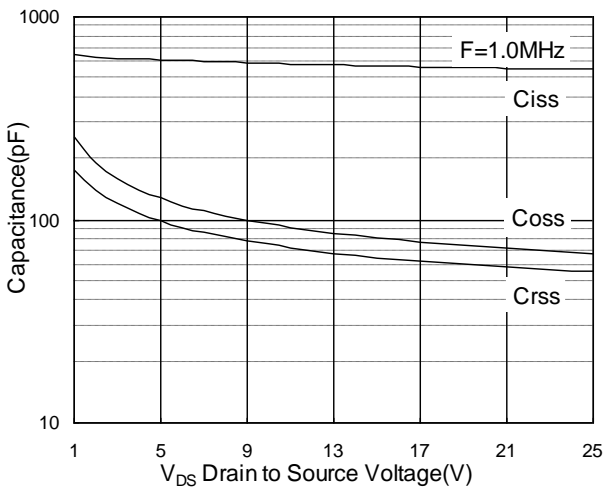
**Fig.4 Gate-Charge characteristics**



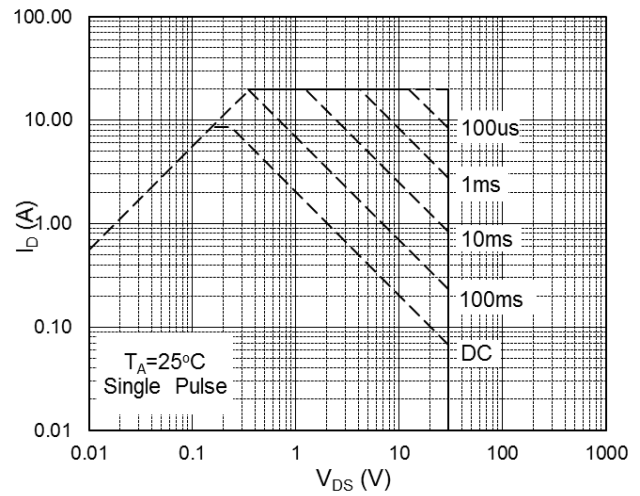
**Fig.5 Normalized V<sub>GS(th)</sub> vs T<sub>J</sub>**



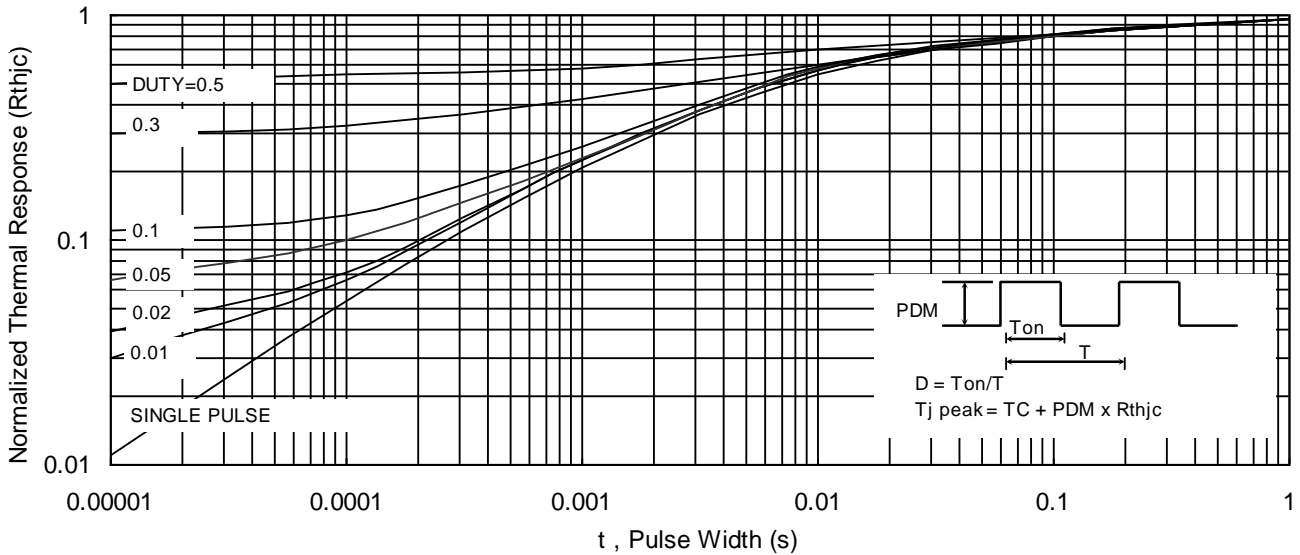
**Fig.6 Normalized R<sub>DSON</sub> vs T<sub>J</sub>**



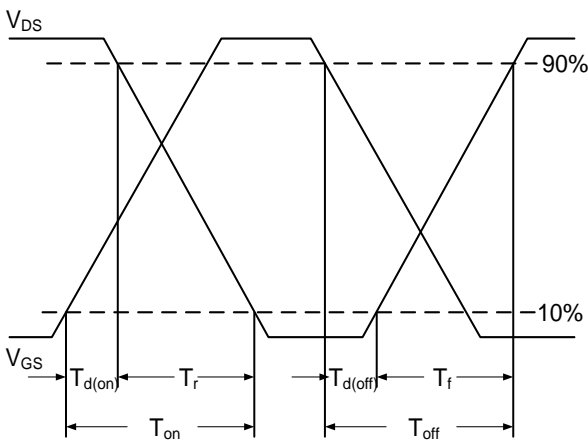
**Fig.7 Capacitance**



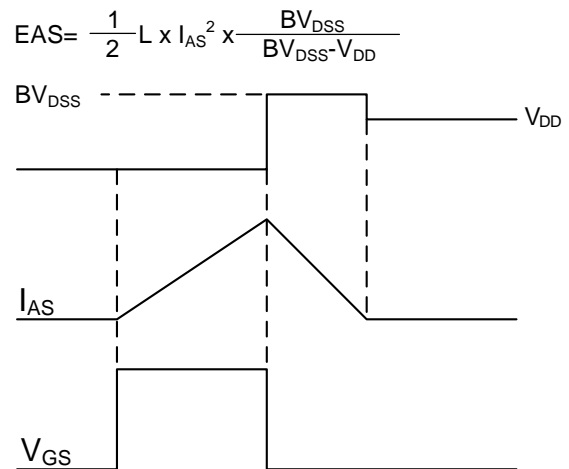
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

**P-Ch Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-30	---	---	V
BV <sub>DSS</sub> Temperature Coefficient	ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Reference to 25°C, I <sub>D</sub> =-1mA	---	-0.021	---	V/°C
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =-10V, I <sub>D</sub> =-7A	---	---	30	mΩ
		V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-5A	---	---	55	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA	-1.0	---	-2.5	V
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub>		---	-4.2	---	mV/°C
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =-24V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	5	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =-5V, I <sub>D</sub> =-7A	---	15	---	S
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	15	30	Ω
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-7A	---	9.8	---	nC
Gate-Source Charge	Q <sub>gs</sub>		---	2.2	---	
Gate-Drain Charge	Q <sub>gd</sub>		---	3.4	---	
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =-15V, V <sub>GS</sub> =-10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =-5A	---	16.4	---	ns
Rise Time	T <sub>r</sub>		---	20.2	---	
Turn-Off Delay Time	T <sub>d(off)</sub>		---	55	---	
Fall Time	T <sub>f</sub>		---	10	---	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-15V, V <sub>GS</sub> =0V, f=1MHz	---	930	---	pF
Output Capacitance	C <sub>oss</sub>		---	148	---	
Reverse Transfer Capacitance	C <sub>rss</sub>		---	115	---	

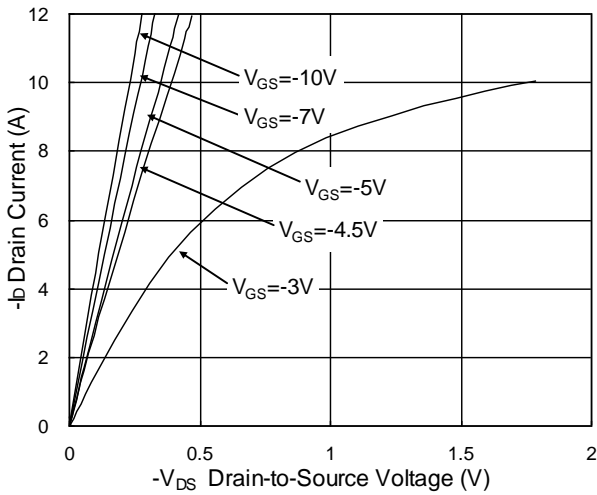
**Drain-Source Diode Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous Source Current <sup>1,5</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	-7.6	A
Pulsed Source Current <sup>2,5</sup>	I <sub>SM</sub>		---	---	-15	A
Diode Forward Voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =-1A, T <sub>J</sub> =25°C	---	---	-1.2	V

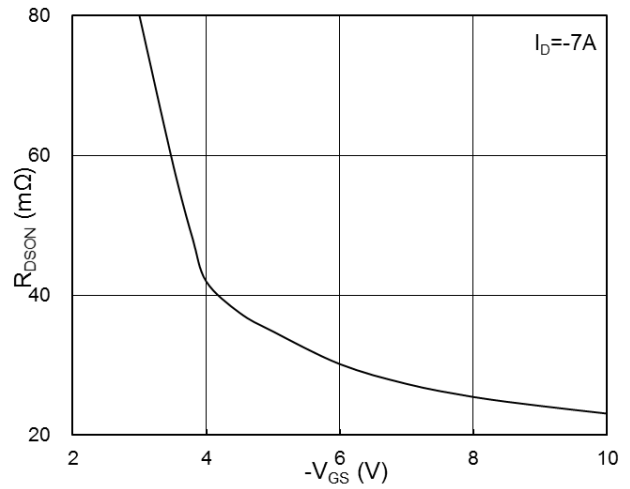
**Note:**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=-25V, V<sub>GS</sub>=-10V, L=0.1mH
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

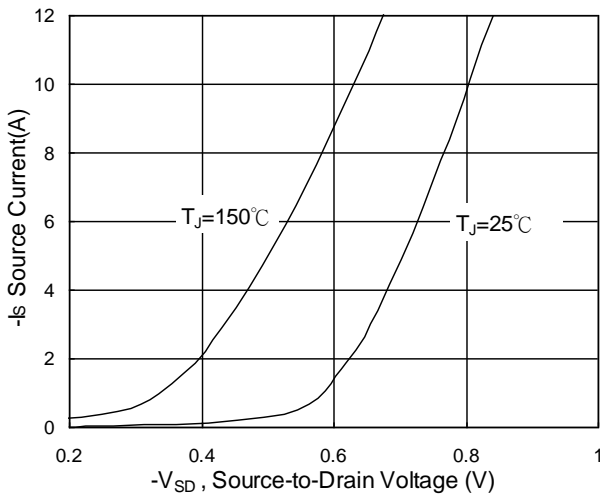
**P-Ch Typical Characteristics**



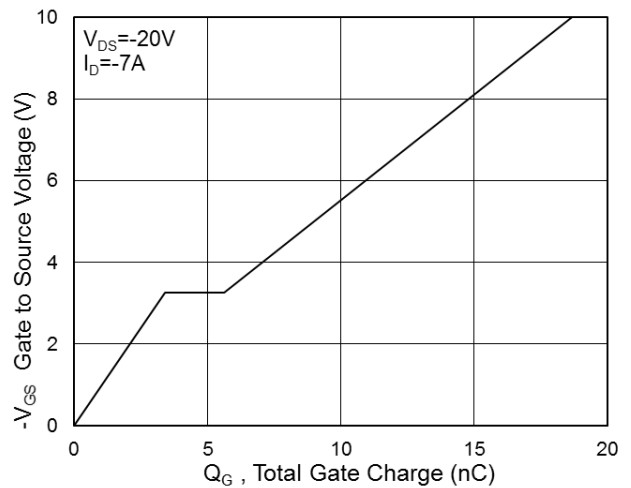
**Fig.1 Typical Output Characteristics**



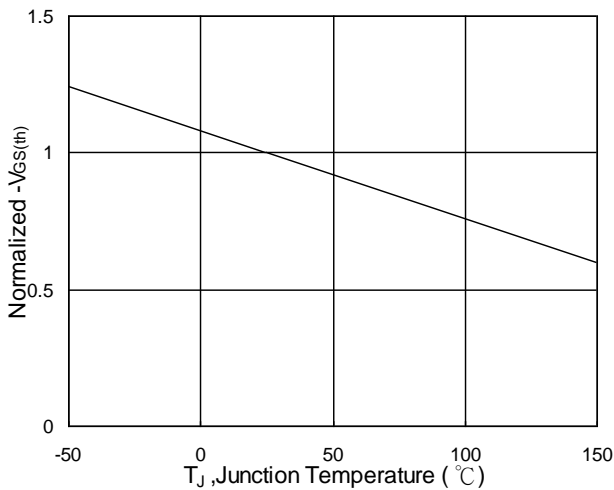
**Fig.2 On-Resistance vs Gate-Source Voltage**



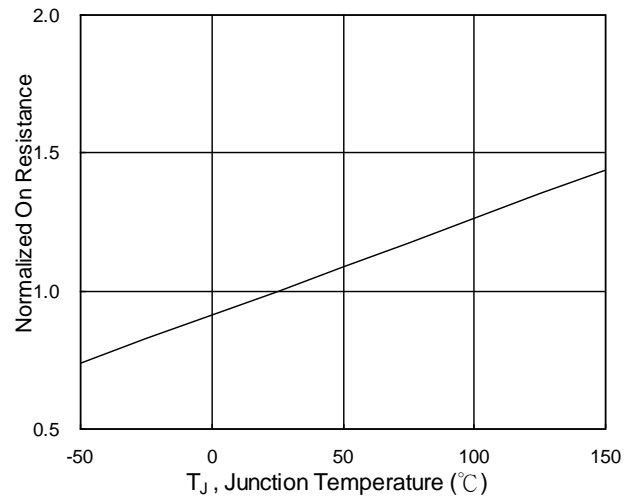
**Fig.3 Forward Characteristics of Reverse**



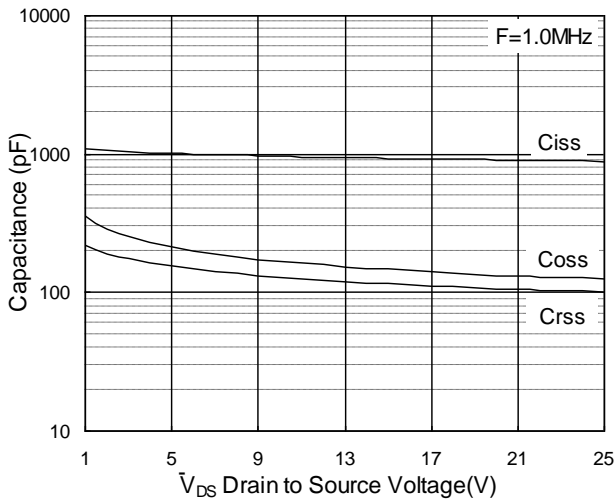
**Fig.4 Gate-Charge Characteristics**



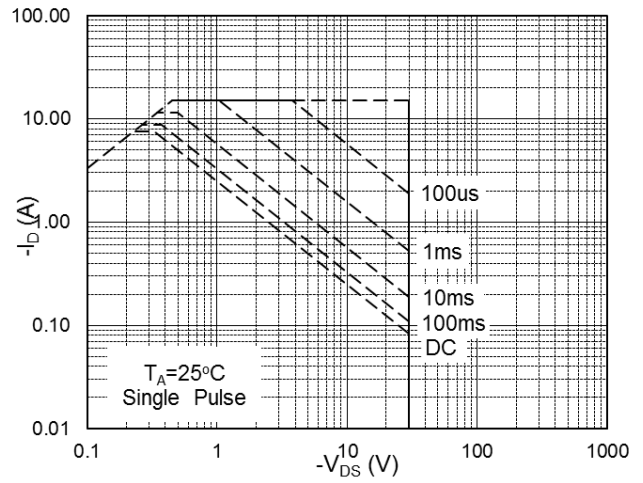
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



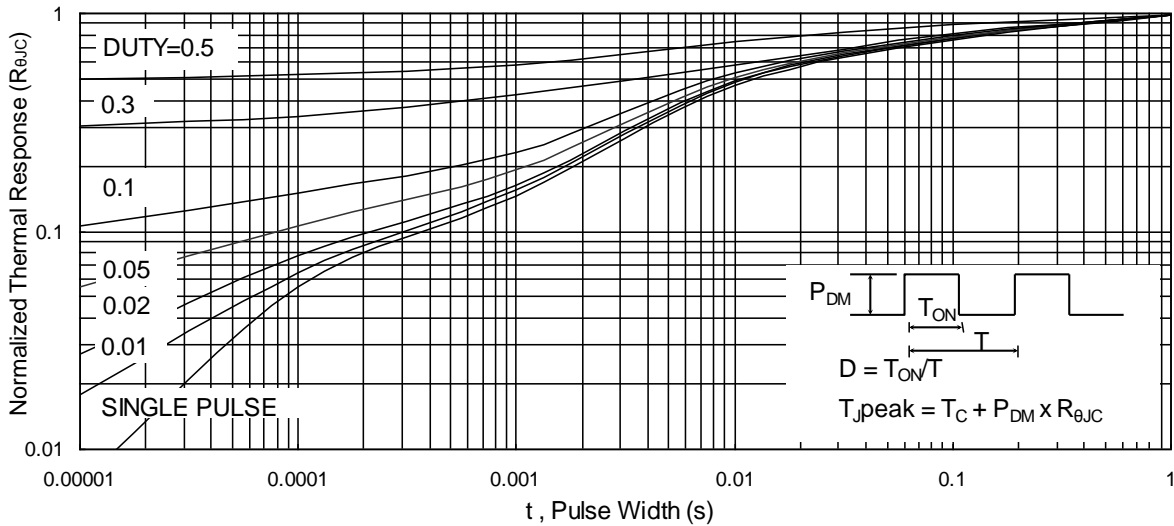
**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



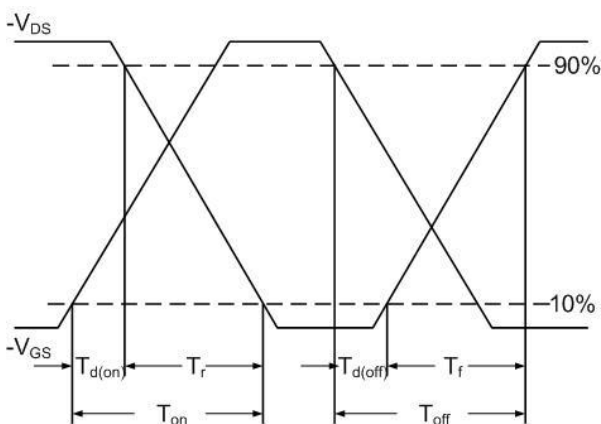
**Fig.7 Capacitance**



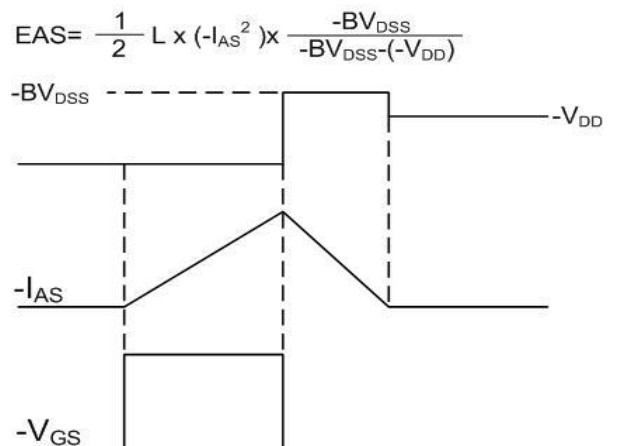
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

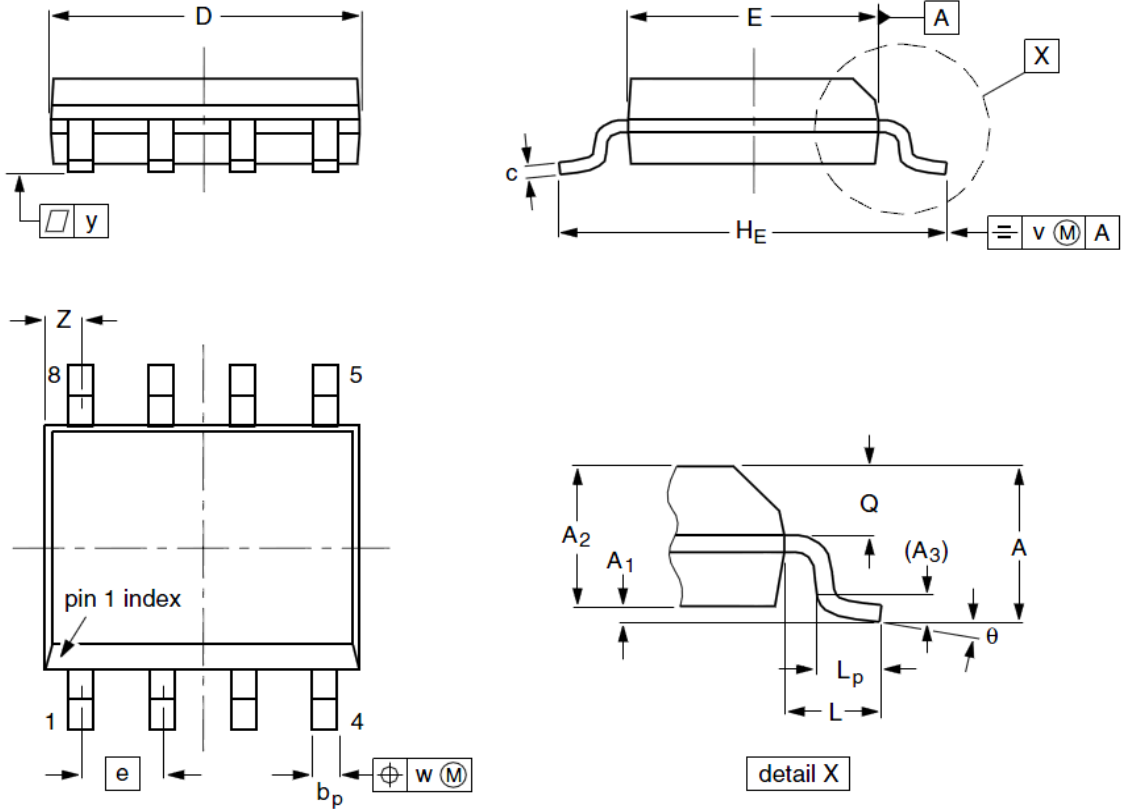


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Waveform**

**SOP-8 Package Outline Dimensions**



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
<b>A</b>	1.35	1.55	1.75	<b>A<sub>1</sub></b>	0.10	0.18	0.25
<b>A<sub>2</sub></b>	1.25	1.45	1.65	<b>A<sub>3</sub></b>	--	0.25	--
<b>b<sub>p</sub></b>	0.36	0.42	0.51	<b>c</b>	0.19	0.22	0.25
<b>D</b>	4.70	4.92	5.10	<b>E</b>	3.80	3.90	4.00
<b>e</b>	--	1.27	--	<b>H<sub>E</sub></b>	5.80	6.00	6.20
<b>L</b>	--	1.05	--	<b>L<sub>p</sub></b>	0.40	0.68	1.00
<b>Q</b>	0.60	0.65	0.73	<b>v</b>	--	0.25	--
<b>w</b>	--	0.25	--	<b>y</b>	--	0.10	--
<b>Z</b>	0.30	0.50	0.70	<b>θ</b>	0°		8°