

**Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

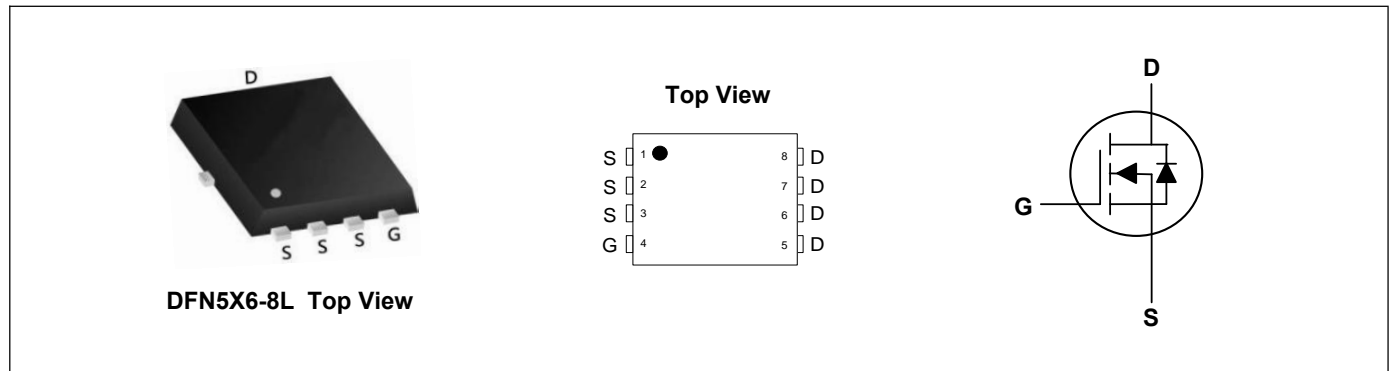
**Product Summary**



$V_{DS}$	100	V
$I_D$	41	A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	15	m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	25	m $\Omega$

**Applications**

- High Frequency Point-of-Load, Synchronous Buck Converter
- Networking DC-DC Power System
- Load Switch



**Absolute Maximum Ratings ( $T_C=25^{\circ}C$ , unless otherwise noted)**

Parameter	Symbol	Rating	Units
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current <sup>1</sup>	$I_D@T_C=25^{\circ}C$	41	A
Continuous Drain Current <sup>1</sup>	$I_D@T_C=100^{\circ}C$	26	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	71	A
Single Pulse Avalanche Energy <sup>3</sup>	EAS	5	mJ
Avalanche Current	$I_{AS}$	10	A
Total Power Dissipation <sup>4</sup>	$P_D@T_C=25^{\circ}C$	46	W
Total Power Dissipation <sup>4</sup>	$P_D@T_C=100^{\circ}C$	19	W
Storage Temperature Range	$T_{STG}$	-55 to 150	$^{\circ}C$
Operating Junction Temperature Range	$T_J$	-55 to 150	$^{\circ}C$

**Thermal Characteristics**

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	---	50	$^{\circ}C/W$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	---	2.7	$^{\circ}C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100	---	---	V
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =12A	---	12.5	15	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =8A	---	19	25	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1	2	3	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V	---	---	1	uA
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =20A	---	22.8	---	S
Gate Resistance	R <sub>g</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =0V, f=1MHz	---	3	---	Ω
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, I <sub>D</sub> =12A	---	22.5	---	nC
Gate-Source Charge	Q <sub>gs</sub>		---	3.2	---	
Gate-Drain Charge	Q <sub>gd</sub>		---	7.6	---	
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =10V, R <sub>G</sub> =3Ω, I <sub>D</sub> =1A	---	6	---	ns
Rise Time	T <sub>r</sub>		---	15	---	
Turn-Off Delay Time	T <sub>d(off)</sub>		---	16	---	
Fall Time	T <sub>f</sub>		---	25	---	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =50V, V <sub>GS</sub> =0V, f=1MHz	---	1055	---	pF
Output Capacitance	C <sub>oss</sub>		---	182	---	
Reverse Transfer Capacitance	C <sub>rss</sub>		---	5	---	

**Drain-Source Diode Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode Forward Voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	---	0.85	1.1	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> =20A, V <sub>R</sub> =50V di/dt=100A/μs, T <sub>J</sub> =25°C	---	40	---	nS
Reverse Recovery Charge	Q <sub>rr</sub>		---	59	---	nC

**Note:**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.1mH
- 4.The power dissipation is limited by 150°C junction temperature

**Typical Characteristics**

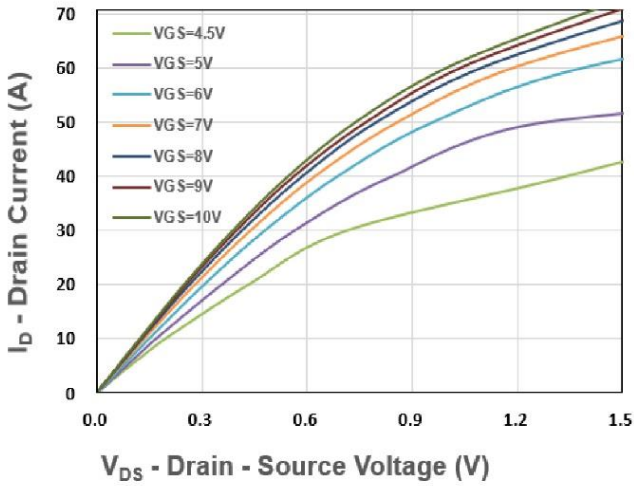


Figure 1. Output Characteristics

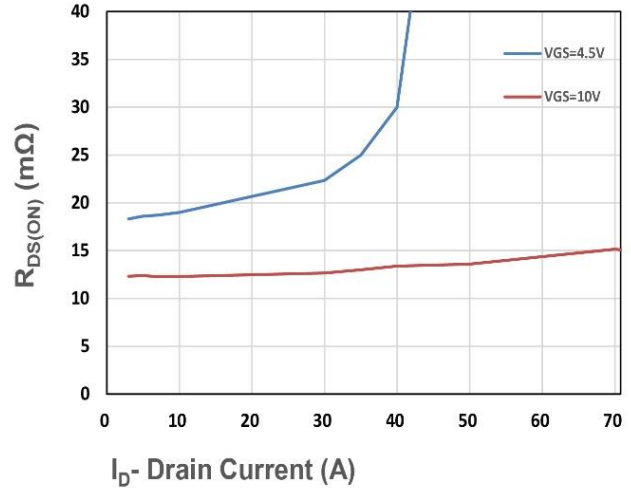


Figure 2. On-Resistance vs.  $I_D$

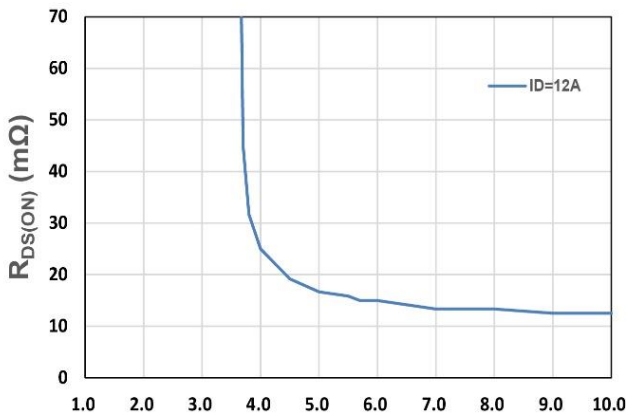


Figure 3. On-Resistance vs.  $V_{GS}$

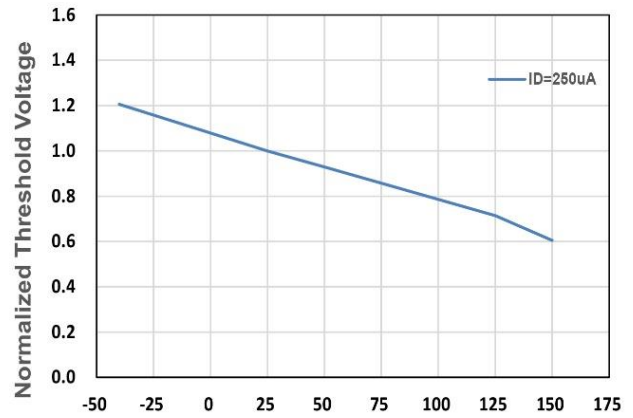


Figure 4. Gate Threshold Voltage

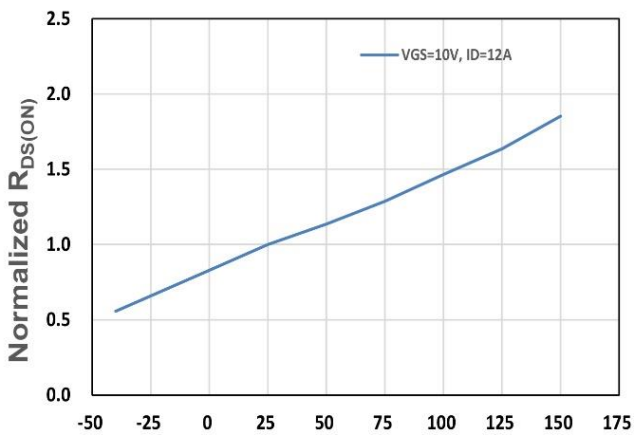


Figure 5. Drain-Source On Resistance

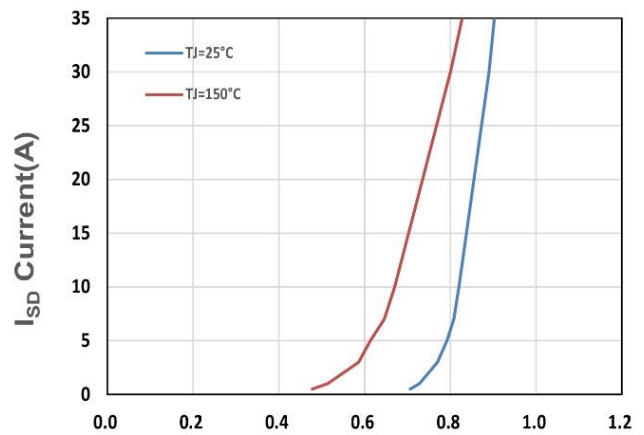
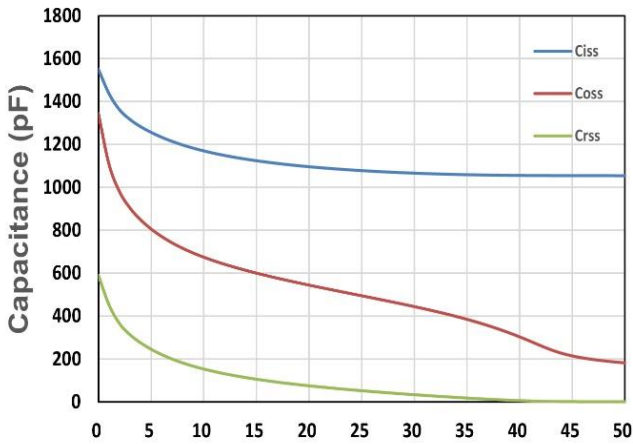
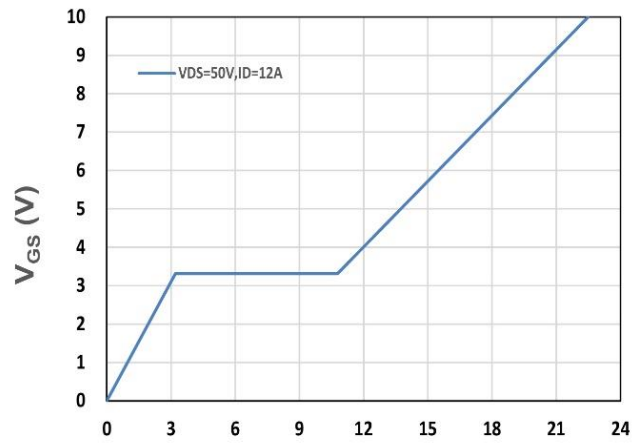


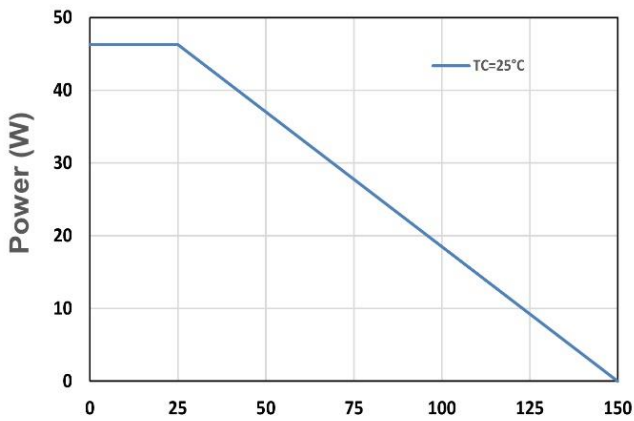
Figure 6. Source-Drain Diode Forward



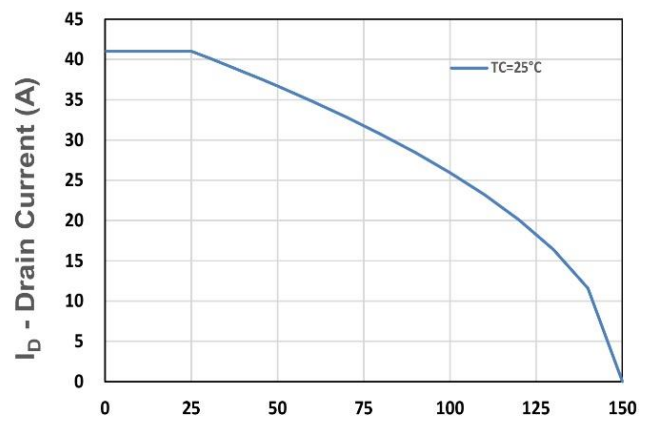
**V<sub>DS</sub> - Drain - Source Voltage (V)**  
Figure 7. Capacitance



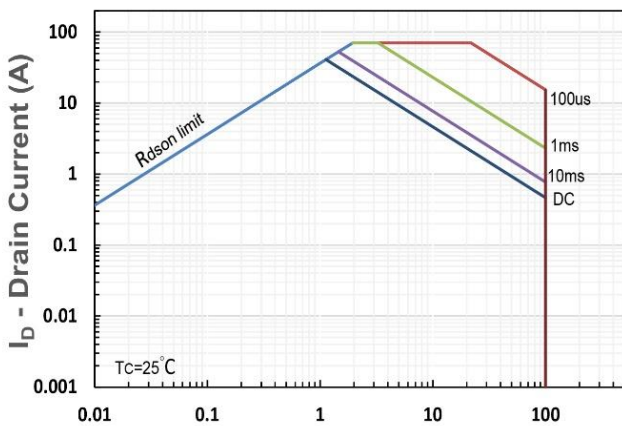
**Q<sub>g</sub>, Total Gate Charge (nC)**  
Figure 8. Gate Charge Characteristics



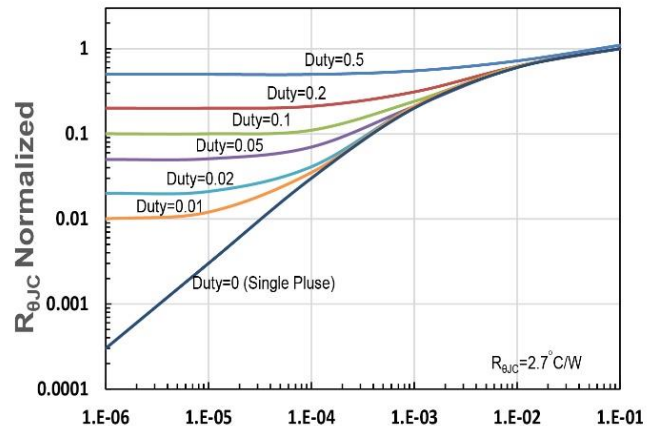
**T<sub>j</sub> - Junction Temperature (°C)**  
Figure 9. Power Dissipation



**T<sub>j</sub> - Junction Temperature (°C)**  
Figure 10. Drain Current

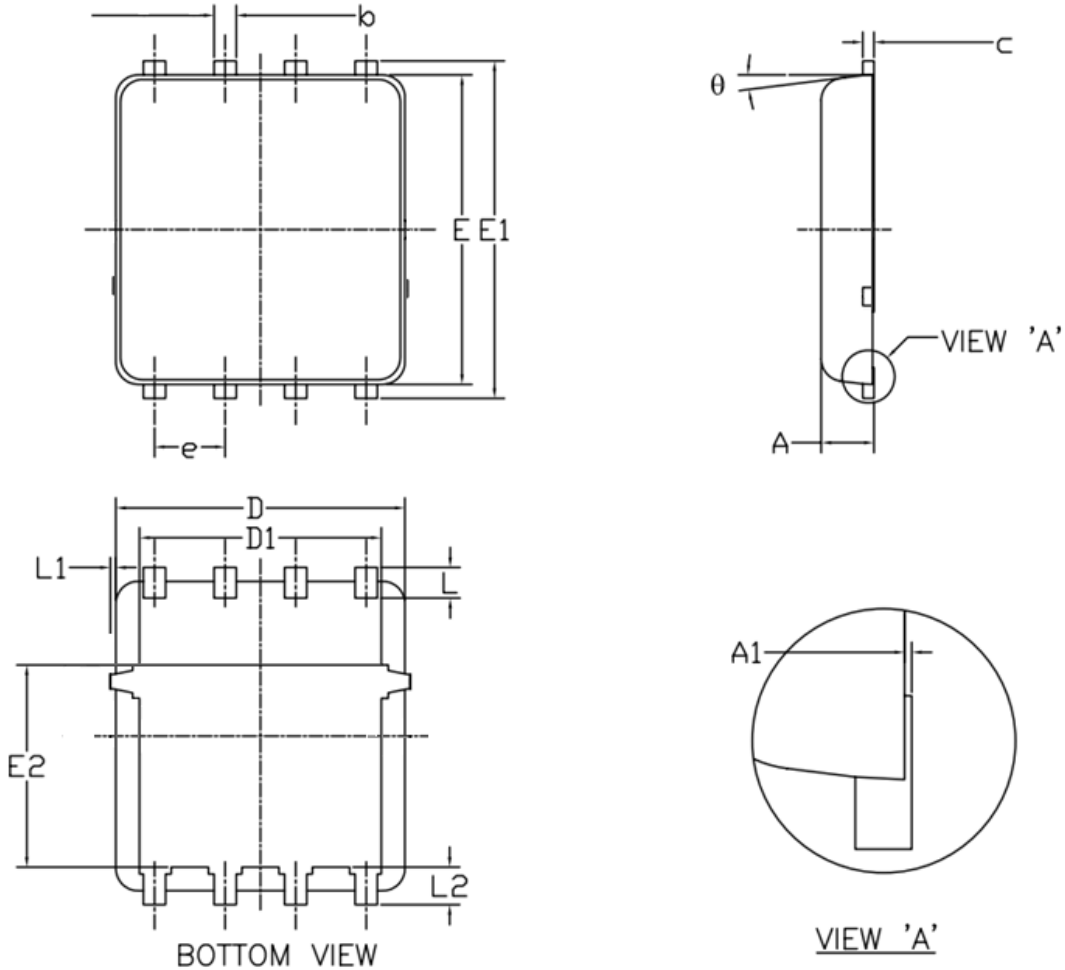


**V<sub>DS</sub> - Drain-Source Voltage (V)**  
Figure 11. Safe Operating Area



**t<sub>1</sub>, Square Wave Pulse Duration(s)**  
Figure 12. R<sub>θJC</sub> Transient Thermal Impedance

**DFN5X6-8L Package Outline Dimensions**



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
<b>A</b>	0.90	1.00	1.20	<b>E1</b>	5.90	6.10	6.35
<b>A1</b>	0.00	--	0.05	<b>E2</b>	3.38	3.58	3.92
<b>b</b>	0.30	0.40	0.51	<b>e</b>	1.27 BSC		
<b>c</b>	0.20	0.25	0.33	<b>L</b>	0.51	0.61	0.71
<b>D</b>	4.80	4.90	5.40	<b>L1</b>	--	--	0.15
<b>D1</b>	3.61	4.00	4.25	<b>L2</b>	0.41	0.51	0.61
<b>E</b>	5.65	5.80	6.06	<b>theta</b>	0°	--	12°