

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

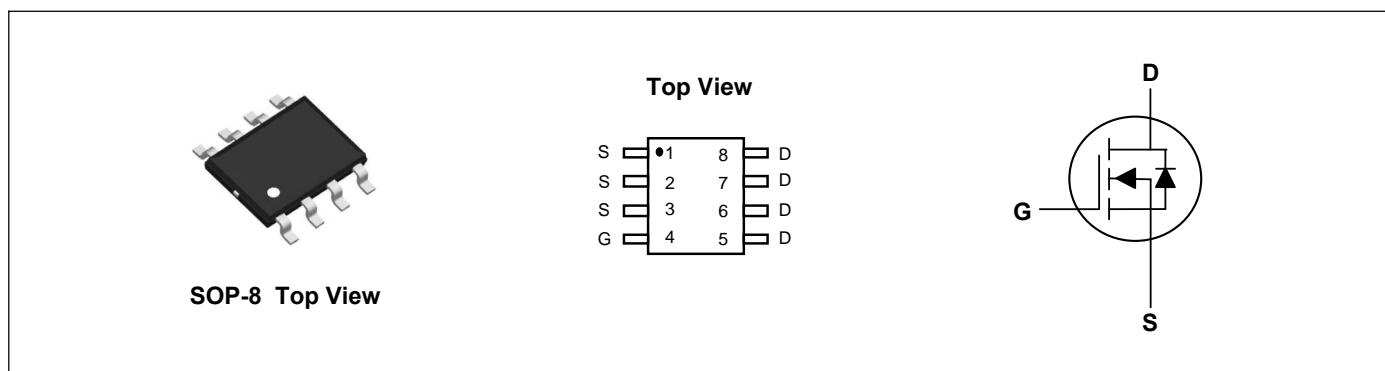
Product Summary



V_{DS}	60	V
I_D	18	A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	6.5	mΩ
$R_{DS(ON)}$ (at $V_{GS}=4.5V$)	8.5	mΩ

Applications

- High Frequency Point-of-Load, Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch



Absolute Maximum Ratings($T_c=25^\circ C$, unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current, $V_{GS} @ 10V^1$	$I_D @ T_A=25^\circ C$	18	A
Continuous Drain Current, $V_{GS} @ 10V^1$	$I_D @ T_A=100^\circ C$	14	A
Pulsed Drain Current ²	I_{DM}	130	A
Single Pulse Avalanche Energy ³	EAS	125	mJ
Avalanche Current	I_{AS}	50	A
Total Power Dissipation ⁴	$P_D @ T_A=25^\circ C$	3.1	W
Storage Temperature Range	T_{STG}	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction-Ambient ¹ ($t \leq 10S$)	$R_{\theta JA}$	---	45	°C/W
Thermal Resistance Junction-Ambient ¹ (Steady State)		---	80	°C/W

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	60	---	---	V
Static Drain-Source On-Resistance ²	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}}=10\text{V}$, $I_D=8\text{A}$	---	---	6.5	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=4\text{A}$	---	---	8.5	$\text{m}\Omega$
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	---	2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{\text{DS}}=60\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^\circ\text{C}$	---	---	5	
Gate-Source Leakage Current	I_{GSS}	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
Forward Transconductance	g_{fs}	$V_{\text{DS}}=5\text{V}$, $I_D=18\text{A}$	---	65	---	S
Total Gate Charge (10V)	Q_g	$V_{\text{DS}}=48\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=18\text{A}$	---	75	---	nC
Gate-Source Charge	Q_{gs}		---	15.5	---	
Gate-Drain Charge	Q_{gd}		---	20.3	---	
Turn-On Delay Time	$T_{\text{d(on)}}$	$V_{\text{DD}}=30\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=18\text{A}$	---	18.5	---	ns
Rise Time	T_r		---	8.8	---	
Turn-Off Delay Time	$T_{\text{d(off)}}$		---	58.8	---	
Fall Time	T_f		---	15.8	---	
Input Capacitance	C_{iss}	$V_{\text{DS}}=25\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	4006	---	pF
Output Capacitance	C_{oss}		---	320	---	
Reverse Transfer Capacitance	C_{rss}		---	222	---	

Drain-Source Diode Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous Source Current ^{1,5}	I_s	$V_G=V_D=0\text{V}$, Force Current	---	---	18	A
Pulsed Source Current ^{2,5}	I_{SM}		---	---	130	A
Diode Forward Voltage ²	V_{SD}	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^\circ\text{C}$	---	---	1.2	V
Reverse Recovery Time	t_{rr}	$I_F=18\text{A}$, $\text{di}/\text{dt}=100\text{A}/\mu\text{s}$, $T_J=25^\circ\text{C}$	---	22.9	---	nS
Reverse Recovery Charge	Q_{rr}		---	11.6	---	nC

Note:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- 3.The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=50\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.1\text{mH}$, $I_{\text{AS}}=50\text{A}$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

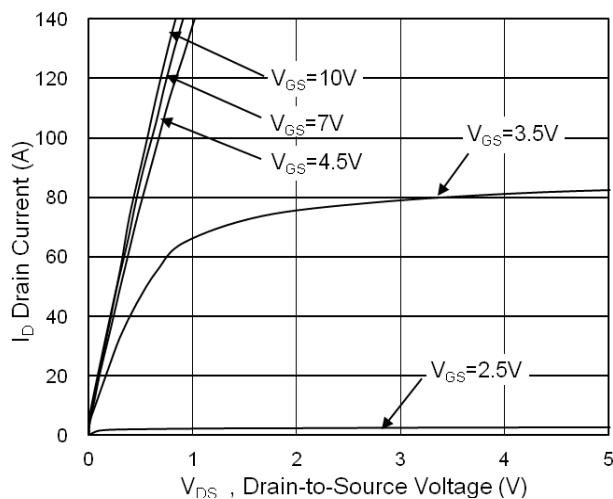


Fig.1 Typical Output Characteristics

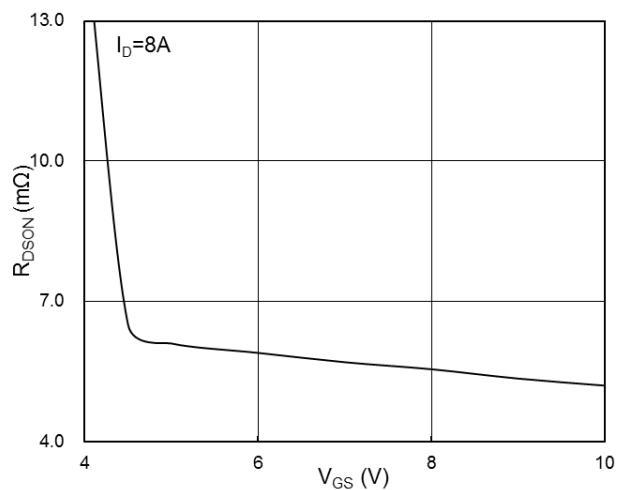


Fig.2 On-Resistance vs. Gate-Source Voltage

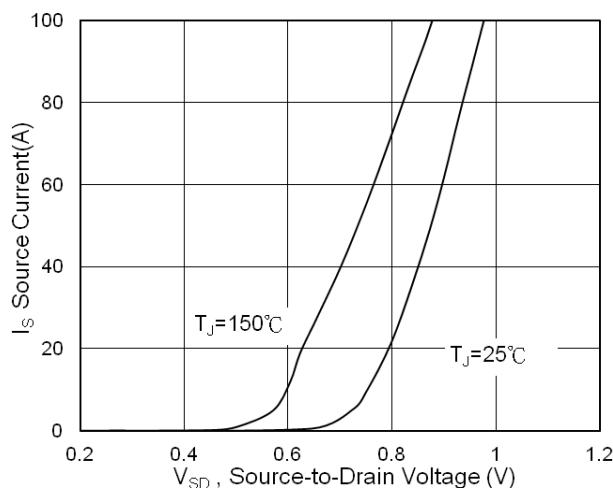


Fig.3 Forward Characteristics of Reverse

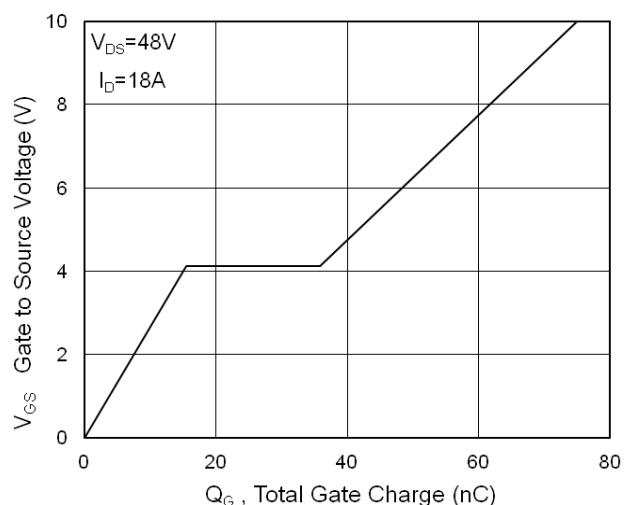


Fig.4 Gate-Charge Characteristics

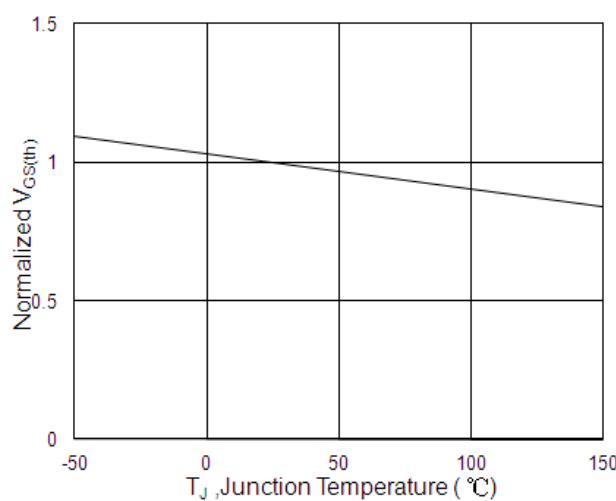


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

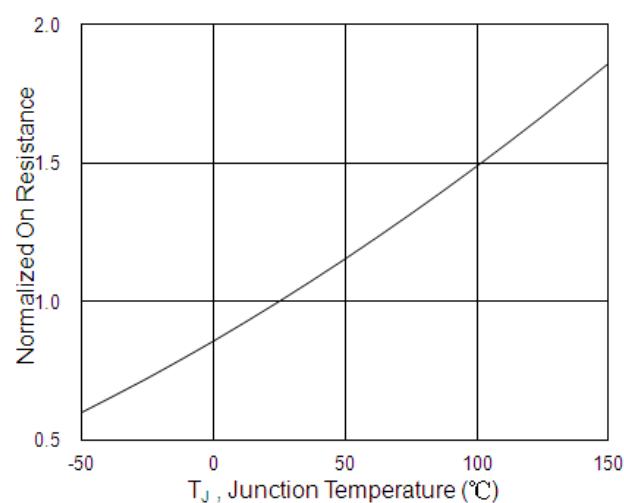
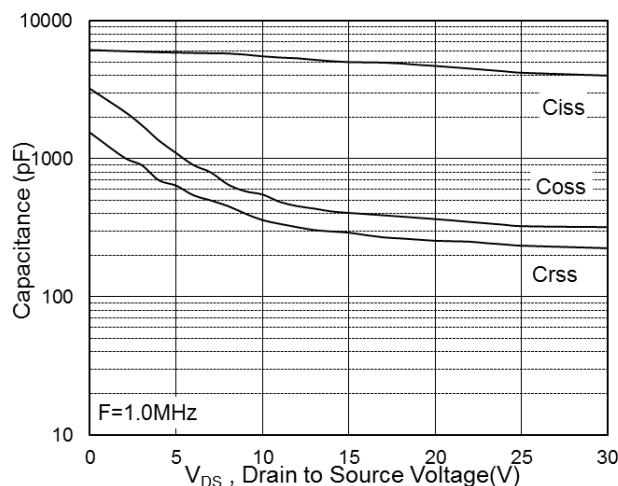
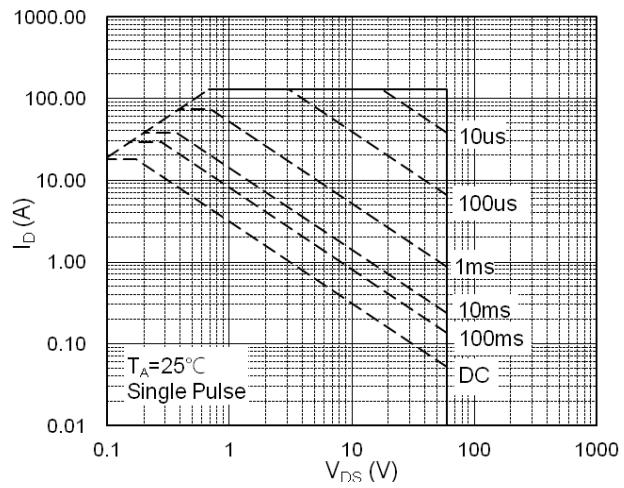
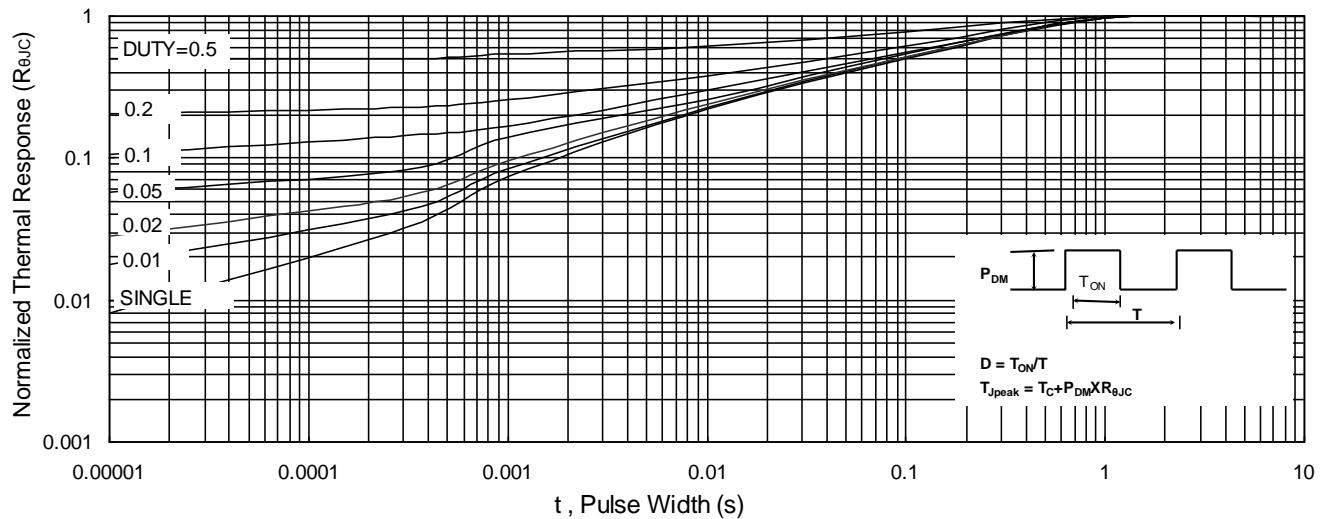
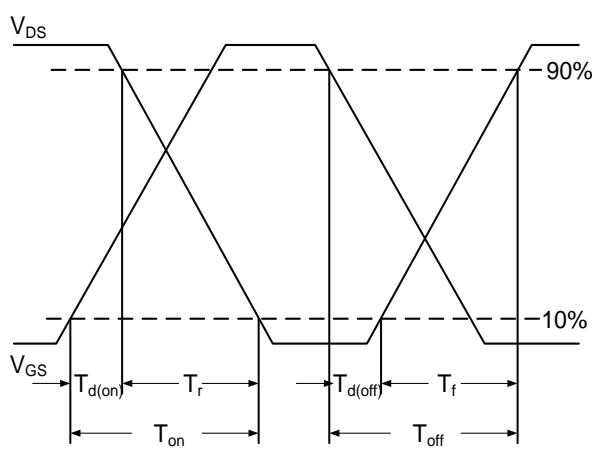
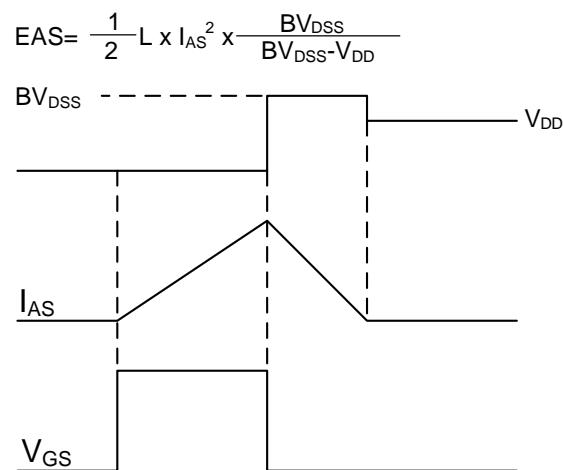
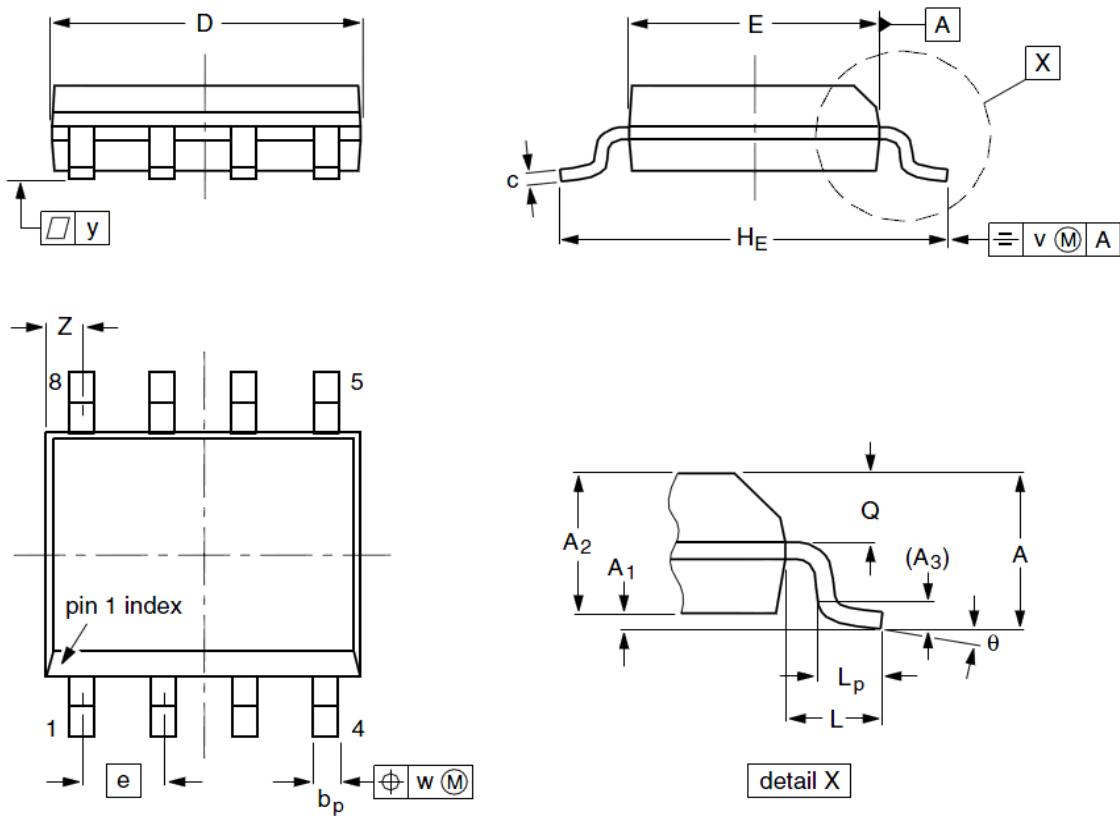


Fig.6 Normalized $R_{DS(on)}$ vs. T_J


Fig.7 Capacitance

Fig.8 Safe Operating Area

Fig.9 Normalized Maximum Transient Thermal Impedance

Fig.10 Switching Time Waveform

Fig.11 Unclamped Inductive Switching Waveform

SOP-8 Package Outline Dimensions



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
A	1.35	1.55	1.75	A₁	0.10	0.18	0.25
A₂	1.25	1.45	1.65	A₃	--	0.25	--
b_p	0.36	0.42	0.51	c	0.19	0.22	0.25
D	4.70	4.92	5.10	E	3.80	3.90	4.00
e	--	1.27	--	H_E	5.80	6.00	6.20
L	--	1.05	--	L_P	0.40	0.68	1.00
Q	0.60	0.65	0.73	v	--	0.25	--
w	--	0.25	--	y	--	0.10	--
Z	0.30	0.50	0.70	θ	0°		8°