

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

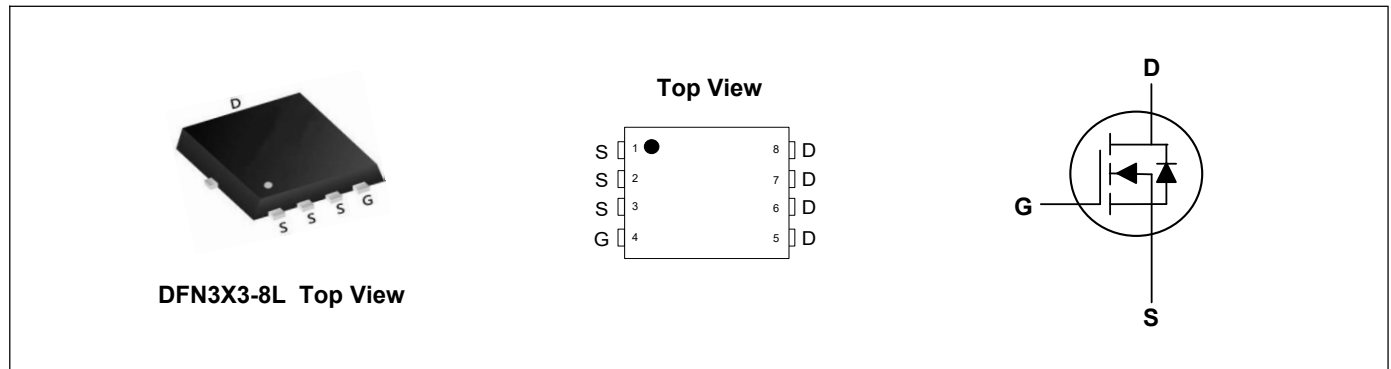
## Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

## Product Summary



$V_{DS}$	40	V
$I_D$	40	A
$R_{DS(ON)}$ (at $V_{GS}=10V$ )	6.5	m $\Omega$
$R_{DS(ON)}$ (at $V_{GS}=4.5V$ )	9	m $\Omega$



## Absolute Maximum Ratings( $T_C=25^{\circ}C$ , unless otherwise noted)

Parameter	Symbol	Rating	Units
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	$I_D@T_C=25^{\circ}C$	40	A
Continuous Drain Current, $V_{GS}$ @ 10V <sup>1</sup>	$I_D@T_C=100^{\circ}C$	31	A
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	140	A
Single Pulse Avalanche Energy <sup>3</sup>	EAS	101	mJ
Avalanche Current	$I_{AS}$	45	A
Total Power Dissipation <sup>4</sup>	$P_D@T_C=25^{\circ}C$	36.7	W
Storage Temperature Range	$T_{STG}$	-55 to 150	$^{\circ}C$
Operating Junction Temperature Range	$T_J$	-55 to 150	$^{\circ}C$

## Thermal Characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal Resistance Junction-Ambient <sup>1</sup>	$R_{\theta JA}$	---	75	$^{\circ}C/W$
Thermal Resistance Junction-Case <sup>1</sup>	$R_{\theta JC}$	---	3.4	$^{\circ}C/W$

**Electrical Characteristics (T<sub>J</sub>=25°C, unless otherwise noted)**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	40	---	---	V
Static Drain-Source On-Resistance <sup>2</sup>	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A	---	5	6.5	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A	---	6.5	9	mΩ
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.0	---	2.5	V
Drain-Source Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	---	---	1	uA
		V <sub>DS</sub> =32V, V <sub>GS</sub> =0V, T <sub>J</sub> =55°C	---	---	5	
Gate-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	---	---	±100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =5A	---	27	---	S
Total Gate Charge (4.5V)	Q <sub>g</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	---	20	---	nC
Gate-Source Charge	Q <sub>gs</sub>		---	5.8	---	
Gate-Drain Charge	Q <sub>gd</sub>		---	9.5	---	
Turn-On Delay Time	T <sub>d(on)</sub>	V <sub>DD</sub> =15V, V <sub>GS</sub> =10V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =1A	---	15.2	---	ns
Rise Time	T <sub>r</sub>		---	8.8	---	
Turn-Off Delay Time	T <sub>d(off)</sub>		---	74	---	
Fall Time	T <sub>f</sub>		---	7	---	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V, f=1MHz	---	2354	---	pF
Output Capacitance	C <sub>oss</sub>		---	215	---	
Reverse Transfer Capacitance	C <sub>rss</sub>		---	175	---	

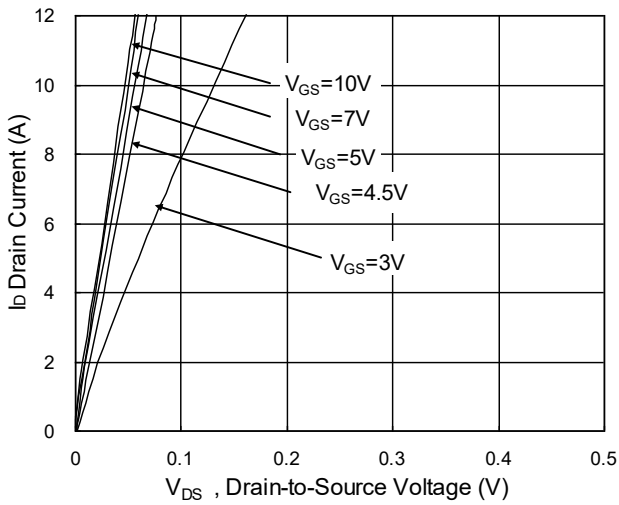
**Drain-Source Diode Characteristics**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Continuous Source Current <sup>1,5</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current	---	---	40	A
Diode Forward Voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =1A, T <sub>J</sub> =25°C	---	---	1	V

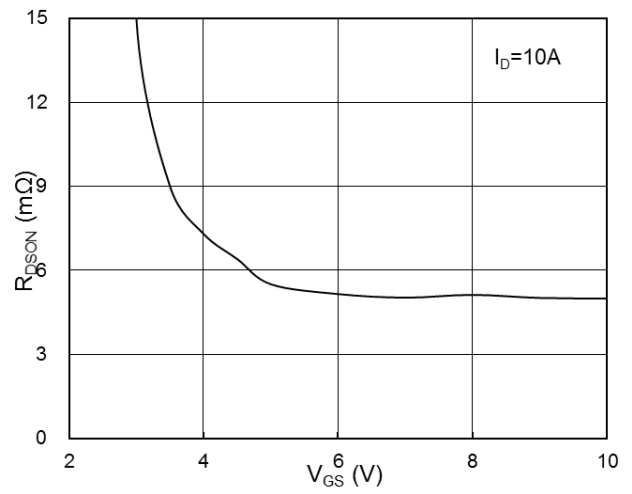
**Note:**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- 3.The EAS data shows Max. rating. The test condition is V<sub>DD</sub>=25V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=45A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation.

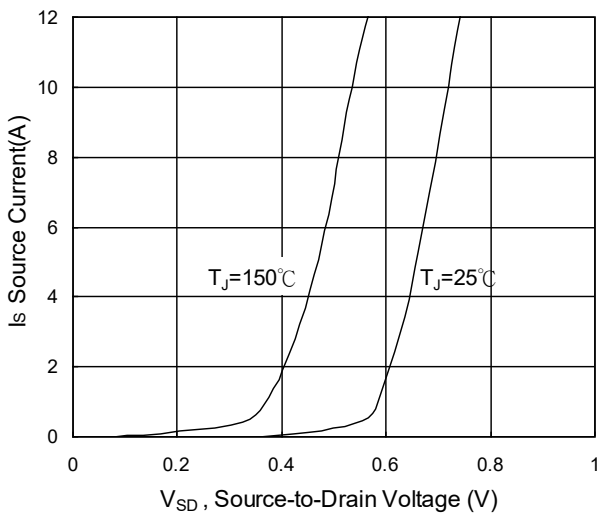
**Typical Characteristics**



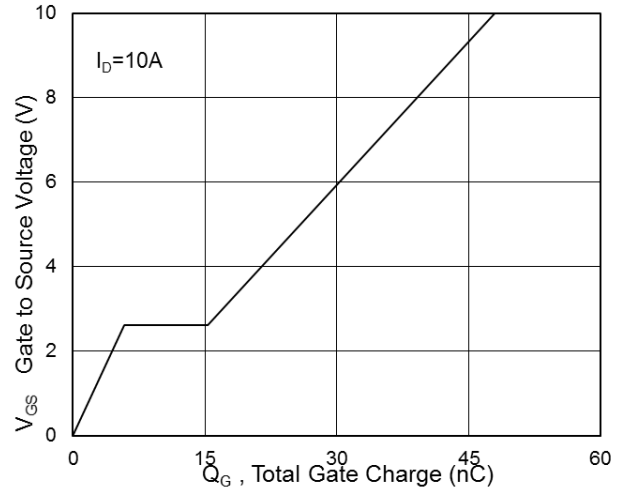
**Fig.1 Typical Output Characteristics**



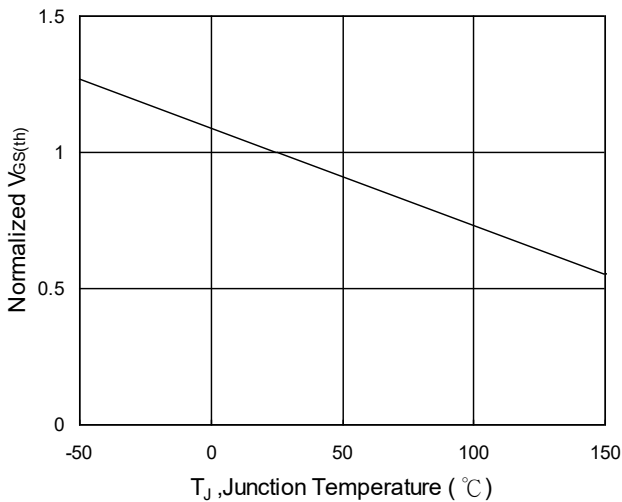
**Fig.2 On-Resistance vs. G-S Voltage**



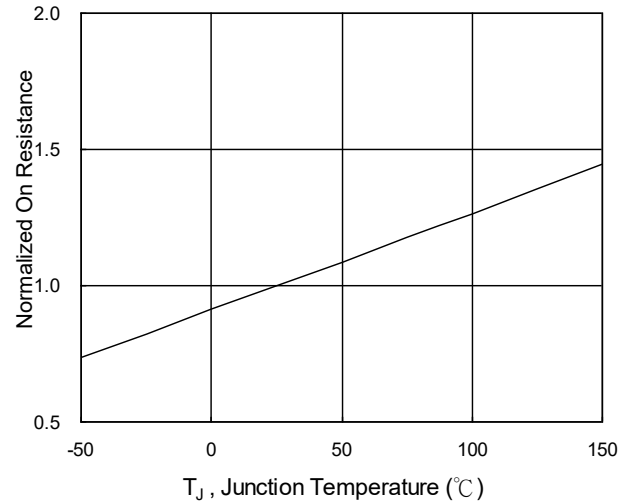
**Fig.3 Source Drain Forward Characteristics**



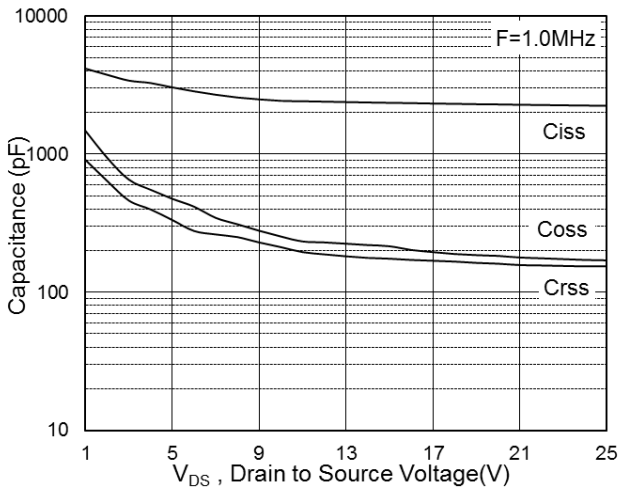
**Fig.4 Gate-Charge Characteristics**



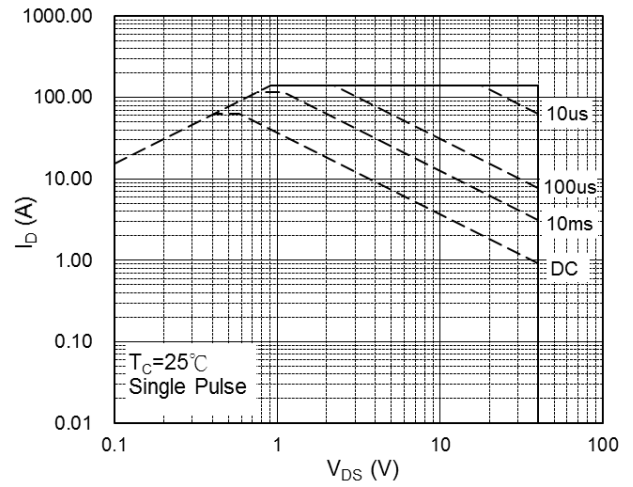
**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



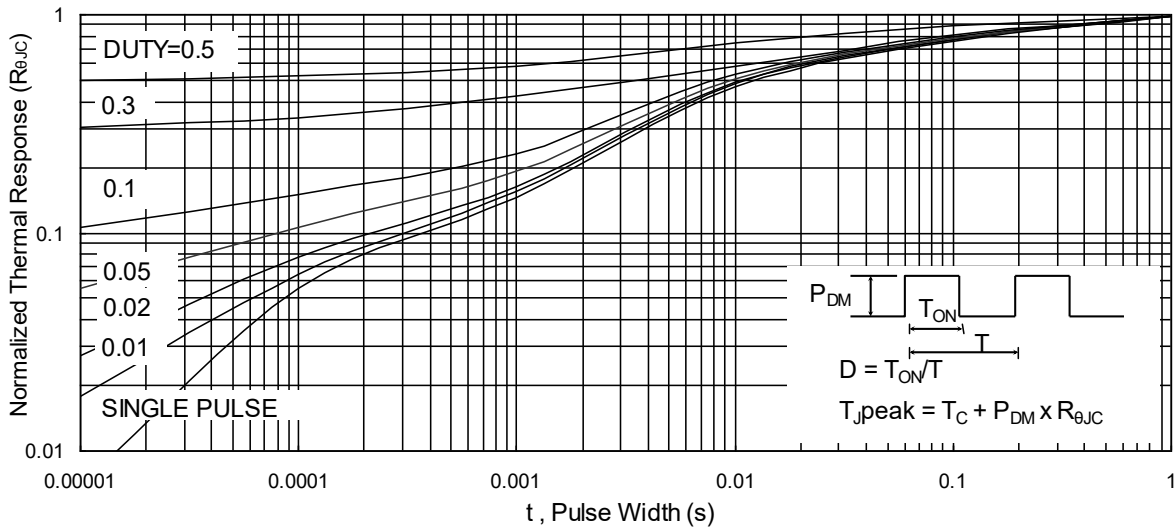
**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**



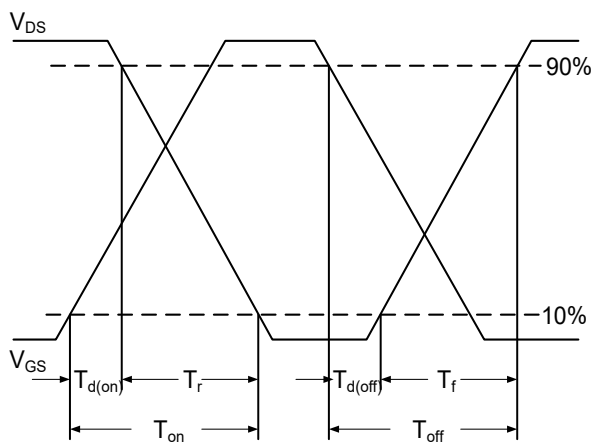
**Fig.7 Capacitance**



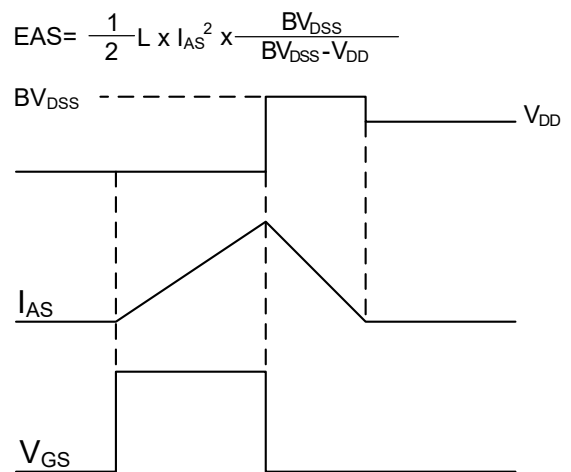
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**

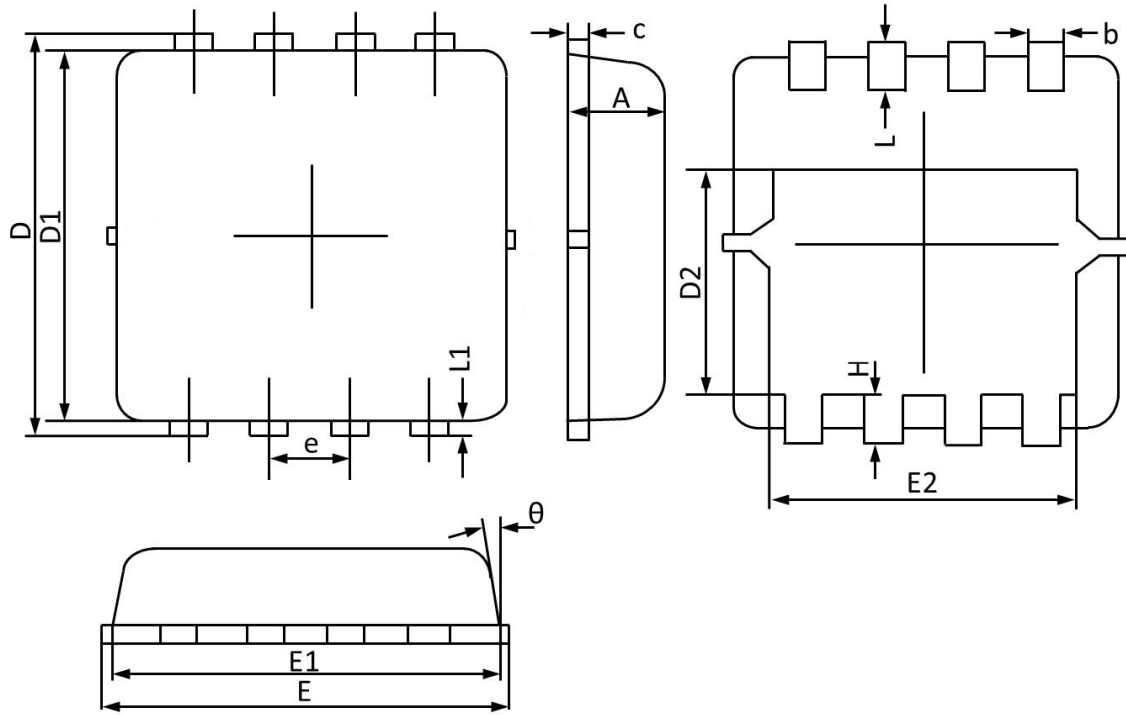


**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Wave**

**DFN3X3-8L Package Outline Dimensions**



Symbol	Dimensions (unit:mm)			Symbol	Dimensions (unit:mm)		
	Min	Typ	Max		Min	Typ	Max
<b>A</b>	0.70	0.75	0.85	<b>E1</b>	2.90	3.10	3.25
<b>b</b>	0.24	0.30	0.35	<b>E2</b>	2.35	2.50	2.60
<b>c</b>	0.10	0.17	0.25	<b>e</b>	0.65 BSC		
<b>D</b>	3.10	3.30	3.45	<b>H</b>	0.30	0.40	0.50
<b>D1</b>	2.90	3.05	3.20	<b>L</b>	0.30	0.40	0.50
<b>D2</b>	1.45	1.70	1.95	<b>L1</b>	--	0.13	--
<b>E</b>	3.05	3.25	3.40	<b>theta</b>	0°		14°